# ADLD Course Project Team-5

Under the guidance of

Dr. Saroja V Siddamal.

|  |  |  |
| --- | --- | --- |
| **Name** | **USN** | **Roll no** |
| T. Maitri | 01FE20BEC120 | 304 |
| Sheela Kapase | 01Fe20BEC094 | 244 |

Statement: Synchronous FIFO with parameterized FIFO depth.

**Introduction:**

**Synchronous FIFO:** First In First Out (FIFO) is a very popular and useful design block for purpose of synchronization and a handshaking mechanism between the modules.

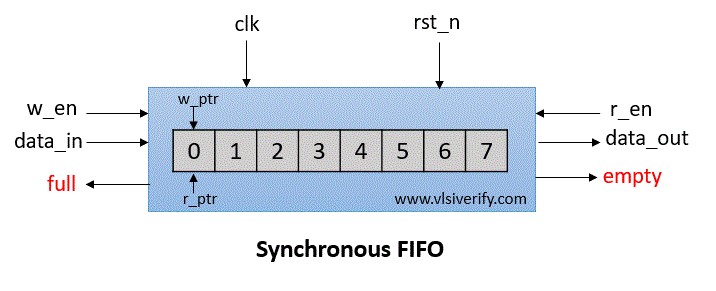
**Depth of FIFO:** The number of slots or rows in FIFO is called the depth of the FIFO.

**Width of FIFO:** The number of bits that can be stored in each slot or row is called the width of the FIFO.

Synchronous FIFO:

In Synchronous FIFO, data read and write operations use the same clock frequency. Usually, they are used with high clock frequency to support high-speed systems.

**Block Diagram:**



Synchronous FIFO operation:

**Signals:** wr\_en: write enable wr\_data: write data

full: FIFO is full

empty: FIFO is empty rd\_en: read enable rd\_data: read data w\_ptr: write pointer r\_ptr: read pointer

Explanation:

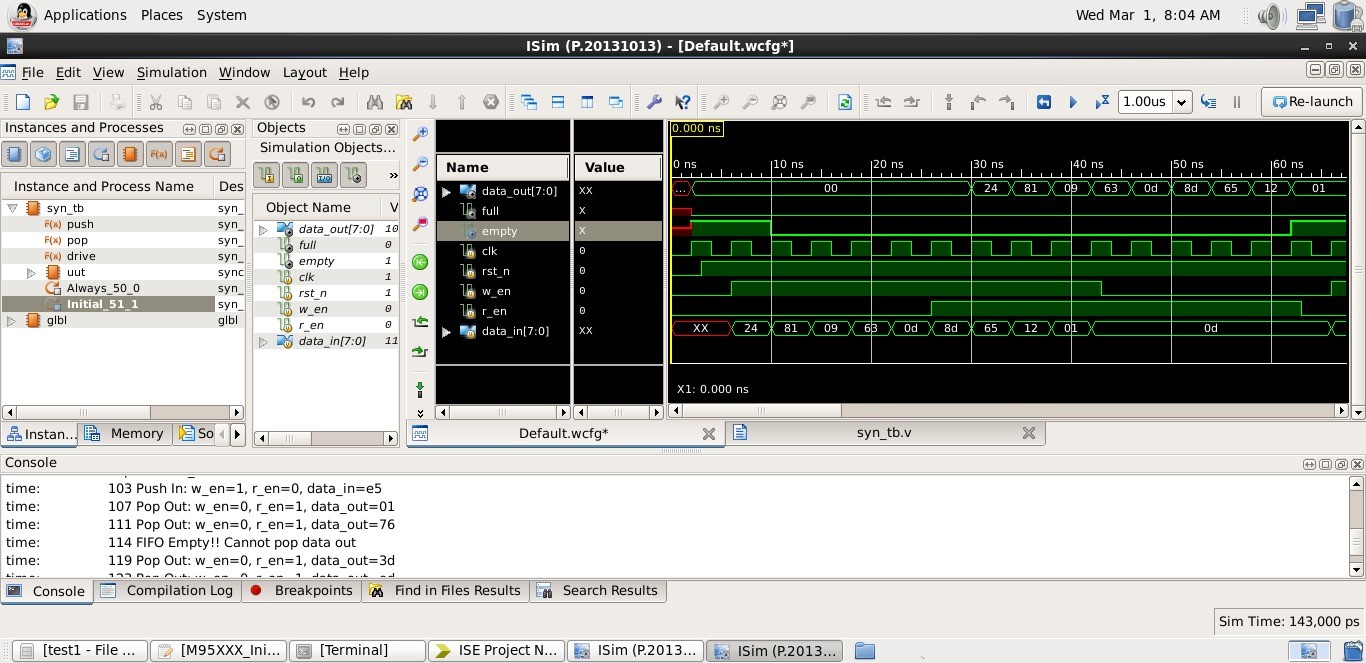
**FIFO write operation:** FIFO can store/write the wr\_data at every pos edge of the clock based on wr\_en signal till it is full. The write pointer gets incremented on every data write in FIFO memory.

**FIFO read operation:** The data can be taken out or read from FIFO at every pos edge of the clock based on the rd\_en signal till it is empty. The read pointer gets incremented on every data read from FIFO memory.

**Empty condition:** Count == 0 i.e. FIFO contains nothing.

**Full condition:**count == FIFO\_DEPTH i.e. counter value has reached till the depth of FIFO

Simulation:



Conclusion:

A parameterized depth synchronous FIFO is that it provides a flexible and efficient way to manage data flow in digital circuits. By allowing the depth of the FIFO to be easily adjusted, it can be optimized for the specific application requirements.

# THANK YOU